ABSTRACT OF THE DISCLOSURE

The present invention provides an efficient method for bypassing outputs while in redundant form to an arithmetic circuit that is capable of adding or subtracting numbers in redundant from and comparing the magnitudes of numbers received in redundant form for equality and inequality relationships. For one embodiment of the invention, an arithmetic circuit subtracts numbers received in redundant form and compares the result to zero represented in redundant form without carry propagation. In parallel with the subtraction and comparison, the most significant bits of each number received in redundant form are generated and compared for equality, and a carry-out is generated for the subtraction. These results are combined by magnitude comparison logic to produce a magnitude comparison for the numbers received in redundant form.